CLAIMS:

1. A filter engine adapted to perform filtering operations on an input data stream comprising blocks of data, the filter engine comprising:

a first memory element adapted to store blocks of data to be processed;

a second memory element adapted to store blocks of data to be processed; and

a single instruction, multiple data (SIMD) processor adapted to receive blocks of data from the first and second memory elements and to simultaneously perform filtering operations on blocks of data from the first and second memory elements.

2. The filter engine of claim 1 wherein the SIMD processor is adapted to receive blocks of data from the first and second memory elements, and to simultaneously perform filtering operations on blocks of data from the first and second memory elements, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the SIMD processor is adapted to receive blocks of data from only one of the first and second memory elements, and to perform filtering operations on the received blocks of data.

3. The filter engine of claim 2 wherein when the filter engine is in the split-operation mode, the m most significant bits of a memory location of the first memory element and the n most significant bits of a memory location of the second memory element are provided to the SIMD processor, and the SIMD processor simultaneously performs filtering operations on the m most significant bits of the memory location of the first memory element and the n most significant bits of the memory location of the second memory element.

4. The filter engine of claim 3 wherein m and n are both equal to t/2, where t is the total number of bits in each of the memory locations of both the first and second memory elements.

5. The filter engine of claim 1 wherein the SIMD processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of data received from the first memory element while the second set of data path units is

simultaneously performing filtering operations on a block of data received from the second memory element.

6. The filter engine of claim 5 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first memory element while the second set of data path units simultaneously performs filtering operations on a block of data received from the second memory element, and wherein when the filter engine is in a non-split-operation mode, both the first and second sets of data path units perform filter operations on blocks of data from only one of the first and second memory elements.

7. The filter engine of claim 6 wherein when the filter engine is in the split-operation mode, the m most significant bits of a memory location of the first memory element are provided to the first set of data path units and the n most significant bits of a memory location of the second memory element are provided to the second set of data path units, and the first set of data path units performs filtering operations on the m most significant bits of the memory location of the first memory element while the second set of data path units simultaneously performs filtering operations on the n most significant bits of the memory location of the second memory element.

8. The filter engine of claim 7 wherein m and n are both equal to t/2, where t is the total number of bits in the memory locations of both the first and second memory elements.

9. The filter engine of claim 1 adapted to perform filtering operations on an input data stream comprising blocks of video data, wherein:

the first memory element is adapted to store blocks of pixel data to be processed;

the second memory element is adapted to store blocks of pixel data to be processed; and

the SIMD processor is adapted to receive blocks of pixel data from the first and second memory elements and to simultaneously perform filtering operations on blocks of pixel data from the first and second memory elements.

10. A filter engine adapted to perform filtering operations on an input data stream comprising blocks of data, the filter engine comprising:

a first memory element adapted to store blocks of data to be processed;

a second memory element adapted to store blocks of data to be processed;

a first shift register adapted to receive and store blocks of data from the first memory element, wherein the first shift register is adapted to selectively shift its contents by a predetermined number of bits corresponding to the size of a data element;

a second shift register adapted to receive and store blocks of data from the second memory element, wherein the second shift register is adapted to selectively shift its contents by a predetermined number of bits corresponding to the size of a data element; and

a processor adapted to receive blocks of data from the first and second shift registers and to simultaneously perform filtering operations on blocks of data from the first and second shift registers.

11. The filter engine of claim 10 adapted to perform filtering operations on an input data stream comprising blocks of video data, wherein the first and second shift registers are adapted to selectively shift their contents by a predetermined number of bits corresponding to the size of one pixel.

12. The filter engine of claim 10 wherein the processor is adapted to receive blocks of data from the first and second shift registers, and to simultaneously perform filtering operations on blocks of data from the first and second shift registers, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory elements, and the processor is adapted to receive blocks of data from the first shift register, but not from the second shift register, and to perform filtering operations on blocks of data from the first shift register.

13. The filter engine of claim 12 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register and the n most significant bits of the second shift register are provided to the processor, and the processor simultaneously performs

filtering operations on the m most significant bits of the first shift register and the n most significant bits of the second shift register.

14. The filter engine of claim 13 wherein m and n are both equal to t/2, where t is the total number of bits that the processor is capable of simultaneously performing filtering operations on.

15. The filter engine of claim 10 wherein the processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of data received from the first shift register while the second set of data path units is simultaneously performing filtering operations on a block of data received from the second shift register.

16. The filter engine of claim 15 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first shift register while the second set of data path units simultaneously performs filtering operations on a block of data received from the second shift register, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory elements, and both the first and second sets of data path units perform filter operations on blocks of data from the first shift register, but not from the second shift register.

17. The filter engine of claim 16 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register are provided to the first set of data path units and the n most significant bits of the second shift register are provided to the second set of data path units, and the first set of data path units performs filtering operations on the m most significant bits of the first shift register while the second set of data path units simultaneously performs filtering operations on the n most significant bits of the second shift register.

18. The filter engine of claim 17 wherein m and n are both equal to t/2, where t is the total number of bits that the plurality of data path units are capable of simultaneously performing filtering operations on.

19. A filter engine adapted to perform filtering operations on an input data stream comprising blocks of data, the filter engine comprising:

a first memory element adapted to store blocks of data to be processed;

a second memory element adapted to store blocks of data to be processed;

a first shift register adapted to receive and store blocks of data from the first memory element, wherein the first shift register is adapted to selectively shift its contents by a predetermined number of bits corresponding to a multiple of the size of a data element;

a second shift register adapted to receive and store blocks of data from the second memory element, wherein the second shift register is adapted to selectively shift its contents by a predetermined number of bits corresponding to a multiple of the size of a data element; and

a processor adapted to receive blocks of data from the first and second shift registers and to simultaneously perform filtering operations on blocks of data from the first and second shift registers.

20. The filter engine of claim 19 adapted to perform filtering operations on an input data stream comprising blocks of video data, wherein the first and second shift registers are adapted to selectively shift their contents by a predetermined number of bits corresponding to a multiple of the size of one pixel.

21. The filter engine of claim 19 wherein the processor is adapted to receive blocks of data from the first and second shift registers, and to simultaneously perform filtering operations on blocks of data from the first and second shift registers, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory elements, and the processor is adapted to receive blocks of data from the first shift register, but not from the second shift register, and to perform filtering operations on blocks of data from the first shift register.

22. The filter engine of claim 21 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register and the n most significant bits of the

second shift register are provided to the processor, and the processor simultaneously performs filtering operations on the m most significant bits of the first shift register and the n most significant bits of the second shift register.

23. The filter engine of claim 22 wherein m and n are both equal to t/2, where t is the total number of bits that the processor is capable of simultaneously performing filtering operations on.

24. The filter engine of claim 19 wherein the processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of data received from the first shift register while the second set of data path units is simultaneously performing filtering operations on a block of data received from the second shift register.

25. The filter engine of claim 24 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first shift register while the second set of data path units simultaneously performs filtering operations on a block of data received from the second shift register, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory elements, and both the first and second sets of data path units perform filter operations on blocks of data from the first shift register, but not from the second shift register.

26. The filter engine of claim 25 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register are provided to the first set of data path units and the n most significant bits of the second shift register are provided to the second set of data path units, and the first set of data path units performs filtering operations on the m most significant bits of the first shift register while the second set of data path units simultaneously performs filtering operations on the n most significant bits of the second shift register.

27. The filter engine of claim 26 wherein m and n are both equal to t/2, where t is the total number of bits that the plurality of data path units are capable of simultaneously performing filtering operations on.